CLAIM LISTING

What is claimed is:

1. (Currently amended) An infrared sensing device, comprising:

~~semiconductor~~ a single-crystal silicon layer ~~substrate~~ having a face;

a readout integrated circuit formed at the face of the silicon layer ~~at said face of said semiconductor substrate~~;

a mesa of Group II - VI semiconductor material epitaxially grown ~~formed~~ on said face of said ~~semiconductor~~ silicon layer ~~substrate~~;

at least one planar photovoltaic infrared detecting cell formed in said mesa; and

a conductor interconnect layer monolithically connecting said infrared detecting cell to said readout integrated circuit.

2. (Currently amended) The infrared sensing device according to claim 1, wherein:

said conductor interconnect layer monolithically connects a common contact ~~cell~~ of said photovoltaic infrared detecting cell lying in one plane to a readout integrated circuit common contact cell lying in another plane, the two planes being separated by a height difference of more than 15 microns.

3. (Original) The infrared sensing device according to claim 1, wherein:

said mesa includes at least two layers of Group II - VI semiconductor material having different band gaps, and

at least one p-n junction diode of said infrared detecting cell being formed in one of said two layers of Group II-VI semiconductor material.

4. (Currently amended) The infrared sensing device according to claim 1, further comprising:

~~a detector output conductively connected to said~~ a first input of the readout integrated circuit ~~input cell~~;

~~a detector common conductively connected to said readout circuit common cell~~an output of the photovoltaic infrared detecting cell;

~~said mesa having~~ at least one sloped side of the mesa; and

at least one conductive trace of the conductor interconnect layer formed on said sloped side connecting said detecting cell~~detector~~ output and said first input of said readout integrated circuit.

5. (Currently amended) The infrared sensing device according to claim ~~3~~4, wherein said sloped side of said mesa has a slope angle between about 40 and 50 degrees relative to ~~a horizontal plane~~ said face.

6. (Currently amended) ~~An Infrared~~ The infrared sensing device of Claim 1, wherein~~,~~ ~~comprising~~:

~~a readout integrated circuit fabricated on a~~ the face of the silicon layer ~~substrate having~~ has a one degree tilt from a (100) crystal direction;~~ and~~

~~a mesa formed on said readout integrated circuit,~~ said mesa including~~:~~

a buffer layer of Group II - VI semiconductor material epitaxially grown on said face;

a first layer of Group II - VI semiconductor material having a first band gap epitaxially grown on said buffer layer;

said buffer layer functionally reducing mismatch between said ~~readout integrated circuit~~ silicon layer and said first layer of Group II - VI semiconductor material;

a second layer of Group II - VI semiconductor material epitaxially grown ~~disposed~~ on said first layer of Group II - VI semiconductor material, said second layer of Group II - VI semiconductor material having a second band gap ~~different from~~ wider than said first band gap;

first and second rows of infrared detecting cells formed in the mesa,

said first row of infrared detecting cells conductively connected to a first row of signal input gates of said readout integrated circuit; and

said second row of infrared detecting cells conductively connected to a second row of signal input gates of said readout integrated circuit.

7. (Currently amended) The i~~I~~nfrared sensing device according to claim 6, wherein said first layer of Group II - VI semiconductor material is formed of indium doped n-type HgCdTe.

8. (Currently amended) The Infrared sensing device according to claim ~~6~~7, wherein the said second layer of Group II - VI semiconductor material is formed of indium doped n-type HgCdTe with a band gap larger than the said first n-type HgCdTe layer.

9. (Currently amended) The Infrared sensing device according to claim 6, wherein said first and second rows of infrared detecting cells include a (p) region formed by the presence of an arsenic compound, the (p) region at least partially extending into said first layer of Group II - VI semiconductor material. ~~layer.~~

10. (Currently amended) An Infrared sensing device having at least one infrared light sensitive element, comprising:

a readout integrated circuit formed at a face of a single-crystal silicon ~~semiconductor~~ layer having a tilt of approximately one degree from the (100) crystal direction;

a mesa epitaxially grown ~~formed~~ on ~~a first surface of said readout integrated circuit~~ the face of the silicon layer, said mesa including:

a buffer layer formed of a Group II - VI material including Cd and Te, the buffer layer epitaxially grown on the silicon layer;

a first layer of Group II - VI semiconductor material epitaxially grown on said buffer layer, said first layer of Group II - VI semiconductor material including Hg, Cd and Te and having a first band gap;

said buffer layer functionally reducing mismatch between said silicon layer ~~readout integrated circuit~~ and said first layer of Group II - VI semiconductor material;

a second layer of Group II - VI semiconductor material including Hg, Cd and Te epitaxially grown ~~disposed~~ on said first layer of Group II - VI semiconductor material, said second layer of Group II -VI semiconductor material having a second band gap; and

said first band gap being ~~different~~ smaller than ~~from~~ said second band gap.

11. (Currently amended) ~~A monolithic infrared detector array according to~~ The infrared sensing device of claim 10, further comprising:

a first infrared detecting cell formed in the mesa and at least partially extending into said first layer of Group II - VI semiconductor material;

a second infrared detecting cell formed in the mesa and at least partially extending into said first layer of Group II - VI semiconductor material, said second infrared detecting cell not overlapping said first infrared detecting cell;

a first conductive interconnect trace formed between said first infrared detecting cell and a first signal input gates of said readout integrated circuit,

a second conductive interconnect trace formed between said second infrared detecting cell and a second signal input gates of said readout integrated circuit,

said mesa having first and second sloped sides;

said first conductive interconnect trace running over said first sloped side of said mesa; and

said second conductive interconnect trace running over said second sloped side of said mesa.

12. (Currently amended) A method for fabricating a monolithic infrared detector, comprising the steps of:

a) providing a wafer with ~~on~~ a read-out integrated circuit ~~a Si~~at a (001) surface of a silicon layer;

b) etching a portion of the Si(001) surface to yield a ~~dyhdride~~ dihydride terminated smooth Si(001) surface, the dihydride terminations providing a passivating layer;

c) after said step of etching, inserting the wafer ~~read-out integrated circuit and clean and passivated Si(001) surface~~ into an MBE chamber;

d) while in the chamber, thermally cleaning, at a temperature at or below 500 °C, said portion of the Si(001) surface to remove the passivating layer;

e ~~d~~) growing a buffer layer of single crystalline CdTe on ~~the ROIC~~ said portion of the ~~silicon layer~~ Si(001) surface within the MBE chamber while maintaining the ~~ROIC~~ wafer at a temperature of less than 500° ~~degrees~~ C;

f ~~e~~) ~~depositing~~ within the same MBE chamber, epitaxially growing a first layer of HgCdTe with narrow band gap on the buffer layer ~~within the MBE chamber~~ while maintaining the wafer ~~ROIC~~ at a temperature of less than 500° ~~degrees~~ C; and

g ~~f~~) ~~depositing~~ within the same MBE chamber, epitaxially growing a second HgCdTe layer with a relatively wider band gap on the first layer of HgCdTe within the MBE chamber while maintaining the ~~ROIC~~ wafer at a temperature less than 500° ~~degrees~~ C.

13. (Currently amended) The method of claim 12, wherein the step of etching comprises the steps of:

b-1) etching the portion of the ~~Si~~ wafer in a diluted solution of HF:H_20 to remove a ~~the~~ passivation layer; and

b-2) etching the Si wafer in a concentrated solution of NH_4F to ~~yield~~ provide said portion ~~a dyhdride terminated smooth Si(001) surface~~ with a passivated layer formed by dihydride terminations.

14. (Currently amended) The method of claim 12, further comprising the steps of:

g) depositing a thin CdTe cap layer on the second HgCdTe layer;

h) coating the entire ~~structure~~ wafer with a photoresist;

i) selectively opening a plurality of windows in the photoresist;

j) fabricating a plurality of p-n junctions in the HgCdTe layers by ~~implementing~~ implanting arsenic atoms through the windows selectively by ion implantation ~~technique~~;

k) annealing the wafer~~ROIC~~ to activate the arsenic;

l) removing the masking photoresist layer;

m) selectively protecting a ~~the~~ grown infrared material structure comprising the buffer layer, the first layer of HgCdTe and the second layer of HgCdTe and the CdTe cap layer as grown on said portion of the silicon layer with a photoresist while leaving the remaining areas of the wafer uncovered;

n) etching the uncovered areas of the wafer to expose ~~the~~ ROIC contact pads of the readout integrated circuit;

o) selectively protecting the grown infrared material structure with a photoresist, leaving the rest of the areas open; and

p) etching the entire ~~sample~~ wafer to produce a mesa structure with a 40 to 50 degree angle between the mesa side walls and ~~horizontal plane~~ the Si(001) surface.

15. (Original) The method of claim 14, wherein a solution of 4% bromine in hydrobromic acid solution is used in the step of etching to produce a mesa structure.

16. (New) A method for fabricating a semiconductor device including silicon and Group II – VI compound semiconductor components, comprising the steps of:

providing a wafer having an elemental silicon layer with a face, an integrated circuit formed at the face of the silicon layer;

etching a portion of the face to yield an epitaxial growth site and to form thereon a dihydride terminated silicon passivation layer;

after said step of etching, inserting the wafer into an MBE chamber;

while in the chamber, thermally cleaning, at a temperature of less than 500° C, the epitaxial growth site to remove the passivation layer; and

after said step of cleaning and while still in the MBE chamber, epitaxially growing a Group II-VI compound semiconductor structure on the epitaxial growth site.